Amendment to the Specification

[0002] This application is also related to the following applications, all filed concurrently herewith and all incorporated herein by reference:

STORAGE SWITCH FOR STORAGE AREA NETWORKS,
Serial No. 10/051,321, filed January 18, 2002;

PROTOCOL TRANSLATION IN A STORAGE SYSTEM,
Serial No. 10/051,415, filed January 18, 2002, now U.S. Pat. No. 7,404,000, issued July 22, 2008;

SWITCH-BASED ~~SERVERLESS~~ STORAGE SERVICES,
Serial No. 10/051,164, filed January 18, 2002, now U.S. Pat. No. 7,185,062, issued February 27, 2007;

PACKET CLASSIFICATION IN A STORAGE SYSTEM
Serial No. 10/051,093, filed January 18, 2002, Notice of Allowance, March 19, 2009;

ENFORCING QUALITY OF SERVICE IN A STORAGE NETWORK,
Serial No. 10/051,339, filed January 18, 2002, now U.S. Pat. No. 7,421,509, issued September 2, 2008;

POOLING AND PROVISIONING STORAGE RESOURCES IN A STORAGE NETWORK,
Serial No. 10/050,974, filed January 18, 2002, now U.S. Pat. No. 6,976,134, issued December 13, 2005; and

LOAD BALANCING IN A STORAGE NETWORK,
Serial No. 10/051,053, filed January 18, 2002, now abandoned.

[0087] CPU. On every linecard there is a processor (CPU) 714, which in one embodiment is a PowerPC 750 Cxe. In one embodiment, CPU 714 connects to each PACE with a 3.2 Gb bus, via a bus controller 715 and a bridge 716. In addition, CPU 714 also connects to each PPU, CAM and TM, however, in some embodiments this

connection is slower at 40 Mbps. Both the 3.2 Gb and 40 Mb paths allow the CPU to communicate with most devices in the linecard as well as to read and write the internal registers of every device on the linecard, download microcode, and send and receive control packets. There may be at least one storage medium in the switch for storing software instructions for controlling the CPU and the PPU to perform the operations disclosed herein for receiving, routing and processing packets for storing and accessing data.